# COURSE DESCRIPTION CARD - SYLLABUS

Course name

PO 6.3.1 Programowanie układów FPGA - EC 6.3.1 FPGA Circuit Programming

## Course

Field of study
Teleinformatics

Year/Semester
3/6

Area of study (specialization)

Profile of study
general academic

Level of study
first-cycle studies

Course offered in
Polish

Form of study
full-time

Requirements
elective

## Number of hours

Lecture
15

Laboratory classes
30

Other (e.g. online)

Tutorials
0

Projects/seminars
0/0

## Number of credit points

3

## Lecturers

Responsible for the course/lecturer:

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Responsible for the course/lecturer:

mgr. Adam Grzelka, ITM, 61 665 3896
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## Prerequisites

A student starting this course should have basic knowledge of digital circuit design and digital simulation. Should have the ability to program in c/c++, use integrated environments programming and obtaining information from indicated sources. Should also understand the need to expand competencies.
In addition, in terms of social competence the student must present such attitudes as honesty, responsibility, perseverance, cognitive curiosity, creativity, personal culture, respect for other people.

## Course objective

1. To provide students with basic knowledge of advanced digital circuit design for programmable circuits, with emphasis on FPGAs.
2. develop students' ability to solve basic design and implementation problems related to programmable circuits.
3. Developing in students the ability to obtain knowledge about current solutions used in programmable systems.

## Course-related learning outcomes

### Knowledge

1. Has knowledge of analysis and synthesis of digital combinatorial and sequential circuits, knows basic digital functional blocks, principles of design of complex digital circuits and their implementation in FPGA technology.
2. Has in-depth knowledge of the design and operation of data communications systems used to provide multimedia services using FPGAs.
3. Has basic knowledge in evaluating parameters of designed FPGA digital circuits as well as computer aided design.

### Skills

1. Is able to analyze and design digital combinational and sequential circuits and digital systems in FPGA technology with given criteria, using appropriate engineering methods and tools.
2. Is able to plan and conduct computer simulations and use programming environments and computer-aided design tools to analyze and evaluate the performance of FPGAs.

### Social competences

1. The student knows the limits of his knowledge and understands the necessity of its updating. Is open to possibilities of continuous education and improvement of professional, personal and social competences.
2. Has a sense of responsibility for the designed information and communication systems and realizes the social risks in case of inadequate design or execution.

## Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Formative Assessment:
(a) For laboratory exercises:

• Based on an assessment of the ongoing progress of the tasks.

Summative Assessment:
a) in the scope of lectures verification of the assumed educational results is realized by:
• an assessment of the knowledge demonstrated in the examination. The exam consists of answering questions and solving problems.
A minimum score of 50% is required to receive a 3.0; 3.5 - 60%; 4.0 - 70%; 4.5 - 80% points; 5.0 - 90% points.
b) in the scope of laboratory exercises, verification of the assumed learning outcomes is realized by:
• substantive evaluation of the performance of laboratory tasks,
• continuous evaluation, every class (oral answers),
• grades received on written tests,
• earning extra points for activity during class.

## Programme content

Lectures:

Gain the ability to program FPGAs using examples from XILINX, ALTRA/INTEL, and LATTICE.

1. Introduce the group of field programmable circuits (FPGAs), their internal structure and functional characteristics.
2. FPGA architectures from various manufacturers.
Demonstration of high-speed I/O interfaces and the use of GTP, GTX, GTH gigabit modules in HD-SDI, SATA, PCI-E, and SerDes in HDMI, FlatLink standards.
4. Design techniques: automata, pipelines.
5. Design techniques: frequency domains. Source-synchronous interface.
6. Design techniques: serial, parallel and distributed arithmetic.
7. FPGAs in embedded systems.
8. Overview of hardware description languages (HDL).
9. Introduction to Verilog.
10. introduction to the SystemVerilog language.

Laboratories:

The module includes laboratory activities using development boards, during which students create hardware descriptions in Verilog languages. The content of these classes consolidates and extends the knowledge provided during lectures. The end result will be the ability to write, run and test hardware modules on an FPGA.

1. Familiarization and mastery of lattice's DIAMOND design environment.
2. Implement a random number generator in Verilog language.
3. Implement a text converter in Verilog language.
4. implementation of a project of a complex system for measuring and presenting ECG signal, consisting of: fullHD resolution video signal generator, communication interface circuits (rotary encoder, keyboard, LEDs), ECG analog interface, control system.

## Teaching methods

1. Lectures: multimedia presentation, supplemented with current examples and additional explanations on the blackboard.
2. Laboratories: solving tasks, programming.

## Bibliography

Basic

S. Palnitkar, Verilog HDL (2nd Edition), Prentice Hall Professional, 3 mar 2003
M. Pawłowski, A. Skorupski, Design of complex digital circuits, WKiŁ, 2010.

Additional

J. Bieganowski, G. Wawrzyniak, Verilog language in FPGA design

## Breakdown of average student's workload

| | Hours | ECTS |
|---|---|---|
| Total workload | 86 | 3.0 |
| Classes requiring direct contact with the teacher | 45 | 2.0 |
| Student's own work (preparation for tests, preparation for laboratory classes, literature studies) | 41 | 1.0 |